CLAIMS

What is claimed is:

1. Structure comprising:

a printed circuit board containing a plurality of component contacts for receipt of electronic components;

a plurality of electrically conductive traces formed on said printed circuit board, each trace being electrically connected to a corresponding one of said component contacts; and

at least one integrated circuit mounted on a selected portion of said printed circuit board and containing a plurality of conductive leads, each of said conductive leads being electrically connected to a corresponding one of said electrically conductive traces formed on said printed circuit board thereby to form an electrically conductive path from each of said conductive contacts to the corresponding conductive leads on said at least one integrated circuit, said at least one integrated circuit being configurable by a user to interconnect selected electrically conductive traces on said printed circuit board to achieve a desired electrical function from the electronic components to be connected to said printed circuit board.

2. Structure as in Claim 1 wherein said printed circuit board contains more than one layer of conductive traces.

3. Structure as in Claim 1 wherein at least some of said plurality of electrical contacts comprise a plurality of holes in said printed circuit board, each hole being appropriate for receipt of a conductive lead of an electronic component.

4. Structure as in Claim 3 wherein the interior surface of each hole is plated with a conductive material.

5. Structure as in Claim 4 wherein the conductive material on the interior of each hole is electrically connected to a corresponding one of said electrically conductive traces.

6. Structure as in Claim 1 including a multiplicity of electronic components mounted on said printed circuit board, each electrical lead of said electronic components each making contact with a corresponding electrical contact selected from said plurality of electrical contacts.

7. Structure as in Claim 6 wherein said at least one integrated circuit chip comprises one integrated circuit chip.

8. Structure as in Claim 1 wherein at least some of said electrical contacts on said printed circuit board comprise pads, each pad being connected to a corresponding one of said plurality of electrically conductive traces formed on said printed circuit board.

9. Structure as in Claim 8 wherein each pad is connected by a conductive lead to a hole formed through said printed circuit board, said hole being plated on its interior surface by a conductive material and said hole being in electrical contact with a corresponding one of said electrically conductive traces formed on said printed circuit board.

10. Structure as in Claim 1 wherein said printed circuit board comprises:

a first portion thereof containing conductive traces for interconnecting electronic components formed thereon without the use of a programmable integrated circuit; and

a second portion thereof containing at least one programmable integrated circuit for interconnecting

electronic components formed on at least said second portion of said printed circuit board.

11. A printed circuit board comprising:

a multiplicity of first electrical contacts formed in said printed circuit board for receipt of the leads of electronic components to be mounted on said printed circuit board;

a corresponding multiplicity of second electrical contacts formed in a selected region of said printed circuit board for receipt of the leads on at least one package of at least one integrated circuit chip to be mounted on the printed circuit board for use in interconnecting selected ones of said multiplicity of first electrical contacts; and

conductive traces formed on said printed circuit board, each conductive trace uniquely interconnecting one first electrical contact to a corresponding second electrical contact.

12. A printed circuit board as in Claim 11 including at least one integrated circuit mounted thereon wherein said at least one integrated circuit comprises a programmable circuit for interconnecting selected conductive traces formed on said printed circuit board thereby to form the electronic components to be contained thereon into a selected electrical circuit.

13. Structure as in Claim 12 including means for testing the state of said at least one programmable integrated circuit to determine the state of the signals on said conductive traces.

14. Structure as in Claim 13 including means for transmitting control signals to said at least one integrated circuit for controlling the configuration of said at least one integrated circuit so as to control the interconnection of the conductive traces formed on said printed circuit

board.

15. Structure as in Claim 14 including at least one programmable integrated circuit mounted on said printed circuit board for interconnecting selected traces formed on said printed circuit board.

16. Structure as in Claim 15 wherein said printed circuit board comprises:

a first portion thereof containing conductive traces for interconnecting electronic components formed thereon without the use of a programmable integrated circuit; and

a second portion thereof containing at least one programmable integrated circuit for interconnecting electronic components formed on at least said second portion of said printed circuit board.

17. A printed circuit board comprising:

a multiplicity of component holes for receipt of leads of electronic components;

a corresponding multiplicity of PIC holes for receipt of the leads on the package or packages of a programmable interconnect chip or chips; and

one or more layers of conductive traces formed on said printed circuit board, each conductive trace uniquely connecting one component hole to one PIC hole.

18. Structure as in Claim 17 wherein said printed circuit board comprises:

a first portion thereof containing conductive traces for interconnecting electronic components formed thereon without the use of a programmable integrated circuit; and

a second portion thereof containing at least one programmable integrated circuit for interconnecting electronic components formed on at least said second portion of said printed circuit board.

19. The method of configuring an electronic system on a printed circuit board comprising the steps of:

creating a computer model of the programmable PC board containing a plurality of component contacts for receipt of the leads of electronic components to be mounted on said printed circuit board, a corresponding plurality of PIC contacts for receipt of the leads of one or more programmable interconnect chips ("PIC") for use in interconnecting selected electronic components and conductive traces, each conductive trace connecting one component contact to one PIC contact;

simulating the placement and routing of select electronic components on the component contacts;

simulating the electrical performance of the system with the electrical components interconnected by the PIC;

interconnecting the electronic components in a desired fashion by configuring the PIC to achieve such interconnection;

determining the system performance and system characteristics with the electronic components so interconnected by simulating and/or testing the system so interconnected; and

repeating the above steps making those changes in placement of electronic components as indicated to be required by the simulation or test results until the above steps yield an electronic system which yields the desired characteristics and functional performance.

Sub A67

20. A programmable interconnect chip for use in interconnecting electronic components formed on a printed circuit board, said chip comprising:

a first set of conductive leads formed in a first direction across the surface of said chip, each of said conductive leads comprising one or more conductive segments, portions of selected ones of said segments being connected to pads on the surface of said

programmable interconnect chip, each of said pads being adapted for contact to a corresponding contact on the printed circuit board;

a second set of conductors formed on said programmable interconnect chip in a second direction not parallel to said first direction, each conductive lead in said second set of conductive leads comprising one or more segments; and

means for electrically interconnecting selected ones of said conductive leads in said first set of conductive leads to one or more of said conductive leads in said second set of conductive leads.

21. Structure as in Claim 20 wherein said programmable interconnect chip comprises:

active transistor in said programmable interconnect chip;

means for electrically connecting selected ones of the segments of conductive leads in said first set of conductive leads and in said second set of conductive leads to programmable transistors in the substrate of said programmable interconnect chip; and

means for programming said programmable transistors in said interconnect chip so as to turn on selected ones of the transistors in said programmable interconnect chip to form desired interconnections between selected contacts on said printed circuit board.

Sub E2

22. Structure as in Claim 20 wherein said means for electrically interconnecting comprise a plurality of interconnect structures, each interconnect structure comprising:

a first conductive layer comprising a portion of the conductive segment of a conductive lead in said first set of leads;

a second conductive layer comprising a portion of the conductive segment of a conductive lead in said

second set of conductive leads; and

dielectric formed between said first conductive lead and said second conductive lead, said dielectric being capable of being made conductive by the application of a selected voltage thereto, thereby to form an electrically conductive path from said conductive segment in said first set of conductive leads to said conductive segment in said second set of conductive leads.

add A7